



UNITED STATES PATENT AND TRADEMARK OFFICE

W
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/819,147	03/27/2001	Indra Laksono	VIXS.0100010	2664
29331	7590	01/11/2006		
TOLER & LARSON & ABEL, L.L.P. 5000 PLAZA ON THE LAKE SUITE 265 AUSTIN, TX 78746			EXAMINER LEE, RICHARD J	
			ART UNIT 2613	PAPER NUMBER

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/819,147

Filing Date: March 27, 2001

Appellant(s): LAKSONO, INDRA

MAILED

JAN 11 2006

Technology Center 2600

J. Gustav Larson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 27, 2005 appealing from the Office action mailed March 10, 2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement that there are no interferences or other appeals that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal is contained in the brief.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

Since the after Final amendment dated May 14, 2004 was entered with the request to cancel claim 62, as communicated by the Examiner in the Advisory Action dated May 25, 2004, claim 62 no longer exists. Therefore, item (A) under the Grounds of Rejections to be Reviewed on Appeal (Section VI) as shown at page 6 of the Brief filed September 27, 2005 should be as follows: Claims 1-4, 6, 10-13, 60, 63, 67, and 68 are rejected under 35 U.S.C. 103 as

Art Unit: 2613

unpatentable over Boyce et al (US Pat. No. 5,635,985) in view of Takahashi et al (US Pat. No. 6,005,623).

There are also some typos with respect to each of the items (B), (C), and (E) under the Grounds of Rejections to be Reviewed on Appeal (Section VI) as shown at pages 6-7 of the Brief filed September 27, 2005, and these items should be corrected as follows. Item (B) should be: Claims 7, 8, 15, 17, 19, and 20 are rejected under 35 U.S.C. 103 as unpatentable over Boyce et al and Takahashi et al, and further in view of Yin et al (Video Transcoding by Reducing Spation Resolution). Item (C) should be: Claims 9, 16, and 18 are rejected under 35 U.S.C. 103 as unpatentable over Boyce et al and Takahashi et al, and further in view of Samad et al (U.S. Pat. No. 5,027,203). Item (E) should be: Claim 61 is rejected under 35 U.S.C. 103 as unpatentable over Boyce et al and Takahashi et al, and further in view of Mougeat et al (U.S. Pat. No. 6,236,683).

(7) Claims Appendix

A substantially correct copy of appealed claims appears on page 28-34 of the Appendix to the appellant's brief. The minor errors are as follows: Since only claims involved in the appeal should be listed in the Appendix, withdrawn claims 22-56 should therefore not be listed in the Appendix.

(8) Evidence Relied Upon

The appellant had failed to provide an Evidence Appendix section in the Brief filed September 27, 2005, as required by 37 CFR 41.37(c). But it is clear from the record that there is no evidence submitted and therefore it is assumed that the appellant meant to include a statement of "NONE".

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10, line 1, wherein the claim claims the MPEG recommendation is indefinite because there are many versions of the MPEG recommendations and the recommends are continuously updated. The scope of the claim limitations cannot change over time, and unless the appellant provides in the remarks section of a response to this Office Action stating the specific MPEG version with the date or a copy of the MPEG recommendation is provided, the claim is considered indefinite.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-4, 6, 10-13, 60, 63, 67, and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyce et al of record (5,635,985) in view of Takahashi et al of record (6,005,623).

Boyce et al discloses a low cost joint HD/SD television decoder as shown in Figures 1 and 2A, and substantially the same system and method as claimed in claims 1-4, 10-13, and 68, comprising substantially the same video decoder (i.e., 120, 122, 124, 128, 129, 131-135, 202, 204, 206, 208 of Figure 2A) to receive a video input stream having one or more first motion

vectors, the video decoder to provide decoded video and the first motion vectors associated with the video input stream (see column 6, lines 18-38); a first memory (116 of Figure 2A) coupled to the video decoder to store the first motion vectors, wherein storing the plurality of motion vectors further storing the plurality of first motion vectors in response to a mode indicator being in a first state (i.e., the receipt of motion vectors in first memory 116 is identified/acknowledged by a mode indicator for further processing, see column 6, lines 18-38); a down scaler (i.e., 126 of Figure 2A, and see column 12, line 43 to column 13, line 42) coupled to receive the decoded video and to provide a scaled video; a second memory (i.e., 118 of Figure 2A) coupled to the video decoder to store a representation of the decoded video, wherein the representation of the decoded video is the decoded video; and wherein the video input is an MPEG data input stream (see column 1); determining a plurality of first motion vectors associated with a compressed first video image (see column 6, lines 18-38); storing a representation of the first video image after the step of determining (i.e., 118 of Figure 2A).

Boyce et al does not particularly disclose, though, the followings:

(a) an encoder coupled to the scaler and the first memory to provide a compressed representation of the scaled video using the first motion vectors saved in the first memory, wherein the video encoder has a vector generation portion that provides second motion vectors based on the first motion vectors saved in the first memory, and generating a compressed second video image based upon one or more second motion vectors and a second video image, wherein the second video image is a scaled representation of the first video image, wherein the scaled representation is a scaled-down representation as claimed in claims 1, 6, 11-13; and

(b) a scaling input to indicate an amount of scaling to be implemented by the scaler; receiving a scaling indicator to indicate an amount of scaling to be applied to the compressed second video image; and wherein the decoder and encoder are part of a transcoder processor as claimed in claims 60, 63, and 67.

Regarding (a) and (b), Takahashi et al discloses a video transcoder as shown in Figures 2A-2D, and teaches the conventional use of an encoder (i.e., 20-25, 25', 26, 27) being coupled to a scaler (i.e., 28, 29 of Figure 2C) and a first memory (i.e., 26 of Figure 2C) to provide a compressed representation of the scaled video using first motion vectors (see column 9, lines 23-44), wherein the video encoder has a vector generation portion that provides second motion vectors based on the first motion vectors (i.e., the first motion vectors provided to scaling circuit 29 as scaled to provide the second motion vectors, see column 9, lines 23-44), generating a compressed second video image based upon one or more second motion vectors and a second video image, wherein the second video image is a scaled representation of the first video image (i.e., as provided by encoder as shown in Figure 2C), wherein a scaling input for indicating an amount of scaling to be implemented by the scaler, the scaled representation is a scaled down representation (see column 9, lines 23-44, column 12, lines 19-26); and wherein the decoder and encoder are part of a transcoder processor (see Figure 2). Therefore, it would have been obvious to one of ordinary skill in the art, having the Boyce et al and Takahashi et al references in front of him/her and the general knowledge of video transcoders, would have had no difficulty in providing the video encoder being coupled to a scaler and a first memory to provide a compressed representation of the scaled video using first motion vectors, the video encoder with a vector generation portion that provides second motion vectors based on the first motion

vectors, wherein the second video image is a scaled representation of the first video image, a scaling input for indicating an amount of scaling to be implemented by the scaler, and a transcoder processor all as taught by Takahashi et al within the system as shown in Figure 2A of Boyce et al for the same well known video transcoding purposes as claimed.

4. Claims 7, 8, 15, 17, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Boyce et al and Takahashi et al as applied to claims 1-4, 6, 10-13, 60, 63, 67, and 68 in the above paragraph (3), and further in view of Yin et al of record (Video Transcoding by Reducing Spatial Resolution).

The combination of Boyce et al and Takahashi et al discloses substantially the same system and method as above, but does not particularly disclose wherein a specific vector of the second motion vectors is based on a plurality of vectors of the first motion vectors, wherein the specific vector of the second motion vectors is based on an average of at least two vectors of the first motion vectors, wherein the step of generating the one or more second motion vectors includes averaging at least a portion of the plurality of first motion vectors to represent a vector in the one or more second motion vectors, wherein a number of vectors in the one or more second motion vectors that represents the second video image is different than a number of vectors in the plurality of first motion vectors that represent the first video image, and wherein the number of vectors in the one or more second motion vectors is less than the number of vectors in the plurality of first motion vectors as claimed in claims 7, 8, 15, 17, 19, and 20. However, Yin et al discloses a video transcoder as shown in Figure 4, and teaches the conventional use of a specific vector of the second motion vectors based on a plurality of vectors of the first motion vectors, wherein the specific vector of the second motion vectors is based on

an average of at least two vectors of the first motion vectors (see Figure 1 and section 3.1), wherein a number of vectors in the one or more second motion vectors that represents the second video image is different than a number of vectors in the plurality of first motion vectors that represent the first video image, and wherein the number of vectors in the one or more second motion vectors is less than the number of vectors in the plurality of first motion vectors (i.e., all the first vectors as shown in Figure 1 are reduced to the single average vector, wherein the single average vector represents the specific vector, and thereby provides the number of vectors in the one or more second motion vectors being less than the number of vectors in the plurality of first motion vectors, see section 3.1). Therefore, it would have been obvious to one of ordinary skill in the art, having the Boyce et al, Takahashi et al, and Yin et al references in front of him/her and the general knowledge of the averaging of motion vectors, would have had no difficulty in providing the specific vector of the second vectors based on a plurality of vectors of the first motion vectors, wherein the specific vector of the second motion vectors is based on an average of at least two vectors of the first motion vectors, wherein a number of vectors in the one or more second motion vectors that represents the second video image is different than a number of vectors in the plurality of first motion vectors that represent the first video image, and wherein the number of vectors in the one or more second motion vectors is less than the number of vectors in the plurality of first motion vectors all as taught by Yin et al as part of the video transcoder processings within the combination of Boyce et al and Takahashi et al for the same well known motion estimation with averaging of motion vectors purposes as claimed.

Art Unit: 2613

5. Claims 9, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Boyce et al and Takahashi et al as applied to claims 1-4, 6, 10-13, 60, 63, 67, and 68 in the above paragraph (3), and further in view of Samad et al of record (5,027,203).

The combination of Boyce et al and Takahashi et al discloses substantially the same system and method as above, but does not particularly disclose wherein a specific vector of the second motion vectors is based on a most frequently occurring vector of the first motion vectors, wherein generating the one or more second motion vectors includes selecting a most frequently occurring vector in a portion of the plurality of first motion vectors to represent a vector in the one or more second motion vectors as claimed in claims 9, 16, and 18. The particular video motion estimations involving the motion vector reduction process of providing the most frequently occurring motion vectors is however old and well recognized in the art, as exemplified by Samad et al (see column 15, line 61 to column 16, line 13). Therefore, it would have been obvious to one of ordinary skill in the art, having the Boyce et al, Takahashi et al, and Samad et al references in front of him/her and the general knowledge of motion vector reductions, would have had no difficulty in providing the motion vector reduction process of providing the most frequently occurring motion vectors as taught by Samad et al for the transcoding system as provided in the combination of Boyce et al and Takahashi et al for the same well known motion estimation refinement purposes as claimed.

6. Claims 57, 58, 64, and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Boyce et al and Takahashi et al as applied to claims 1-4, 6, 10-13, 60, 63, 67, and 68 in the above paragraph (3), and further in view of Vainsencher (6,005,624).

The combination of Boyce et al and Takahashi et al discloses substantially the same system and method as above, but does not particularly disclose wherein the first memory comprises a hard drive, wherein the first memory coupled to the video decoder is to store all motion vectors used to build a frame of the video input stream, wherein storing the first motion vectors includes storing the first motion vectors on a hard drive, and wherein the plurality of first motion vectors include all motion vectors used to build a frame of the compressed first video image as claimed in claims 57, 58, 64, and 65. However, Vainsencher discloses a system for performing motion compensation as shown in Figures 1-3, and teaches the conventional use of a memory (112 of Figure 3) coupled to a video decoder (i.e., 102, 104, 106, 108, 110 of Figure 3) to store all plurality of first motion vectors used to build a frame of the compressed video image (see column 8, lines 33-67). It is noted that though Vainsencher teaches that the memory 112 is a SDRAM memory (see column 8, lines 55-57), and not a hard drive memory as claimed. But, Vainsencher does teach the particular use of a hard drive 90 of Figure 2 within the encoder and decoder computer system. It is however considered obvious that such hard drive memory of Vainsencher may certainly be used for storing the motion vectors in place of the SDRAM memory. Therefore, it would have been obvious to one of ordinary skill in the art, having the Boyce et al, Takahashi et al, and Vainsencher references in front of him/her and the general knowledge of motion vector storages, would have had no difficulty in providing the memory 112 for storing all plurality of motion vectors used to build a frame of the compressed video image as

Art Unit: 2613

taught by Vainsencher as well as the obvious use of hard drive 90 of Vainsencher for storing the motion vectors over the SDRAM 112 of Vainsencher for the transcoding system as provided in the combination of Boyce et al and Takahashi et al for the same well known storage of motion vectors within a hard drive system for building frames of video data purposes as claimed.

7. Claim 61 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Boyce et al and Takahashi et al as applied to claims 1-4, 6, 10-13, 60, 62, 63, 67, and 68 in the above paragraph (3), and further in view of Mougeat et al (6,236,683).

The combination of Boyce et al and Takahashi et al discloses substantially the same system and method as above, further including wherein the video decoder is to receive the video input stream has a first set of motion vectors representing a first frame of video (i.e., as provided by 1 of Figure 2B of Takahashi et al), where the one or more first motion vectors being at least a portion of the first set of motion vectors and a second set of motion vectors representing a second frame of video (i.e., scaling circuit 29 provides the second set of motion vectors, see column 9, lines 23-44 of Takahashi et al).

The combination of Boyce et al and Takahashi et al does not particularly disclose wherein the first memory coupled to the video decoder to simultaneously store the first set of motion vectors and the second set of motion vectors as claimed in claim 61. However, Mougeat et al discloses an image predictor as shown in Figures 3, 4, and 6, and teaches the particular use of double buffering of motion vectors wherein motion vectors are simultaneously being stored in memory 40 of Figures 3, 4, 6 (see column 2, lines 22-38, column 2, line 66 to column 4, line 19). Therefore, it would have been obvious to one of ordinary skill in the art, having the Boyce et al, Takahashi et al, and Mougeat et al references in front of him/her and the general knowledge of

double buffering memories, would have had no difficulty in providing the simultaneous storage of motion vectors as taught by Mougeat et al for the motion estimation system within the combination of Boyce et al and Takahashi et al for the same well known parallel processing of data storage purposes as claimed.

(10) Response to Argument

Regarding the appellant's arguments at pages 7-12 of the Brief filed September 27, 2005 concerning in general that Boyce fails to disclose or suggest a first memory coupled to a video decoder and an encoder for the storage of motion vectors provided by the video coder for subsequent use by the encoder as recited in claim 1, and specifically that "... the Boyce reference fails to disclose or suggest the storage of motion vectors in either of the coded data buffer 116 or the rame buffer 118 ... The only reference to motion vectors during the decoding process in the Boyce refdrene discloses that "[t]he preparser 112 parses the incoming bitstream, without performing a complete variable length decode operation, ... to identify MPEG coding elements such as macroblocks including motion vectors and DCT coefficients associated with each of the identified frames in the received data stream." Id., col. 6, lines 17-26. This passage provides only that the motion vectors are identified by the preparser 112 and does not indicate that the motion vectors are stored by the preparser 112 in the coded data buffer 116. The Appellant submits that the preparser 112 presumably identifies the MPEG coding elements, including the motion vectors, for the purpose of discarding the MPEG coding elements ... ", the Examiner respectfully disagrees. As stated by the appellant, the preparser 112 of Boyce et al parses the incoming bitstream to identify MPEG coding elements such macroblocks including motion vectors and DCT coefficients (see column 6, lines 18-38), and the coded data which includes the

motion vector and DCT coefficient data are stored in buffer 116 for further decoding processings. This is evident as shown at column 11, lines 51-65 of Boyce et al wherein it is taught that the motion vectors received as part of the video data stream supplied to the preparser is used by the MPC circuit 130 after buffering of the motion vectors. Though the preparser 112 of Boyce et al may limit the number of DCT coefficients (see column 6, lines 39-58) used to represent a macroblock thereby reducing the storage of the amount of data within coded data buffer 116, the DCT coefficient data and motion vectors are necessarily stored in the coded data buffer 116 before further processings within the syntax parser and VLD circuit 120 and MCT circuit 130 (see column 8, lines 58-63, column 11, lines 51-65). It is further submitted that Takahashi et al nevertheless teaches a video transcoding system as shown in Figures 2B and 2C, and Takahashi et al provides substantially the same if not the same encoder (i.e., 20-25, 25', 26, 27) being coupled to a scaler (i.e., 28, 29 of Figure 2C) and a first memory (i.e., 26 of Figure 2C) to provide a compressed representation of the scaled video using first motion vectors (see column 9, lines 23-44). The encoder of Takahashi et al may certainly be provided within the system as shown in Figure 2A of Boyce et al for carrying out the intended video transcoding operation, and thereby rendering obvious the claimed invention.

Regarding the appellant's arguments at pages 12-13 of the Brief filed September 27, 2005 concerning in general that "... Moreover, the Boyce reference teaches that the "downsampled frames supplied by the frame buffer 118 to the MCP circuit 130 are upsampled ... interpolated and then downsampled prior to generating predictions based on the motion vectors. In this manner the motion vectors which were originally generated based on the full resolution video frames are effectively applied to downsampled video frames ... Thus, the Boyce reference

teaches motion estimation by upsampling and interpolation, thereby rendering the original motion vectors redundant. The storage of redundant or unused information, such as the original motion vectors, in the coded data buff 116 would only result in needlessly occupying space in the coded data buffer 116, and thus, the storage of the original motion vectors in the coded data buffer 116 by the preparser 1112 would be contrary to the teachings of the Boyce reference ...”, the Examiner respectfully disagrees. As pointed out in the above, the motion vectors are necessarily stored in the coded data buffer 116 before further processings within the syntax parser and VLD circuit 120 and MCT circuit 130 (see column 8, lines 58-63, column 11, lines 51-65). Boyce et al at column 11, lines 51-65 teaches that the motion vectors received as part of the video data stream supplied to the preparser is used by the MPC circuit 130, and it is clear as shown in Figure 2A of Boyce et al that the motion vectors are buffered within buffer 116 before being supplied to the MPC circuit 130.

Regarding the appellant’s arguments at page 13 of the Brief filed September 27, 2005 concerning in general that “... Even if, arguendo, the Boyce reference disclosed the storage of the motion vectors in the coded data buffer 116, it will be appreciated that the coded data buffer 116 is coupled to the input of the purported video decoder of Figure 2A of the Boyce reference, so the purported video decoder cannot provide the first motion vectors as recited by claim 1 ...”, the Examiner respectfully disagrees. The motion compensation prediction, i.e. MCP circuit 130, which is part of the video decoder of Boyce et al nevertheless provides motion vectors as a result of the prediction (see column 13, lines 48-63).

Regarding the appellant’s arguments at page 13 of the Brief filed September 27, 2005 concerning Claim 11 and in general that Boyce fails to disclose or suggest a first memory to

Art Unit: 2613

store motion vectors, the Examiner wants to point out that such arguments have been addressed in the above.

Regarding the appellant's arguments at pages 13-16 of the Brief filed September 27, 2005 concerning in general that "... The Takahashi reference neither discloses nor suggest that this side information is stored in memory between the variable length decoder 11 and the scaling circuit 29. According, the Takahashi reference neither discloses nor suggest the limitation of a first memory coupled to store first motion vectors from a video decoder as recited by claim 1 or the limitations of storing a plurality of motion vectors and generating one or more second motion vectors based on the stored plurality of first motion vectors as recited by claim 11 ...", the Examiner respectfully disagrees. Column 9, lines 23-44 of Takahashi et al clearly teaches the side information, which includes motion vector data, is being provided to scaling circuit 29 so as to be used for coding within the coder as shown in Figure 2C. And since the first motion vectors are provided to scaling circuit 29 so as to provide second motion vectors (see column 9, lines 23-44), Takahashi et al renders obvious the features of a "video encoder has a vector generation portion that provides second motion vectors based on the first motion vectors" and "generating one or more second motion vectors based on the stored plurality of first motion vectors". It is submitted again that Takahashi et al provides substantially the same if not the same encoder (i.e., 20-25, 25', 26, 27) being coupled to a scaler (i.e., 28, 29 of Figure 2C) and a first memory (i.e., 26 of Figure 2C) to provide a compressed representation of the scaled video using first motion vectors (see column 9, lines 23-44), and the encoder as shown in Figure 2C generates a compressed second video image based upon one or more second motion vectors and a second video image, wherein the second video image is a scaled representation of the first video image.

Art Unit: 2613

And it is again that the encoder of Takahashi et al may certainly be provided within the system as shown in Figure 2A of Boyce et al for carrying out the intended video transcoding operation, thereby rendering obvious the claimed invention.

Regarding the appellant's arguments at pages 16-18 of the Brief filed September 27, 2005 concerning in general that there is no motivation to combine the Boyce and Takahashi references since the Boyce and Takahashi references focus on solving different problems, the Examiner wants to point out that though Boyce et al and Takahashi et al may teach various features that are different from the present invention, it is still nevertheless that Boyce et al and Takahashi et al renders obvious the claimed invention as explained in the above.

Regarding the appellant's arguments at pages 18-20 of the Brief filed September 27, 2005 concerning the rejection of claims 7-9, 15-20, 57, 58, 64, and 65 under 35 USC 103, and in general that the respective references do not disclose each and every limitation recited by claims 1 and 11, from which these respective claims depend from, the Examiner respectfully disagrees for the above reasons.

Regarding the appellant's arguments at pages 20-23 of the Brief filed September 27, 2005 concerning in general that "... The Appellant disagrees and submits that the Vainsencher reference fails to disclose or even suggest the use of a hard drive as recited by claims 57 and 64 ... No passage of the Vainsencher reference discloses or suggests that motion vectors, or any other video data for that matter, may be stored in the hard drive ... the use of the hard drive 90 for the storage of motion vectors as proposed by the Final Action not only would be contrary to the goal of "guaranteed performance characteristics" sought by the Vainsencher reference but would also be contrary to conventional MPEG processing systems where RAM storage of video

data is standard ...the use of a hard drive to store motion vectors would cause substantial delays due to the latency involved with access to the hard drive ...”, the Examiner wants to point out again that Vainsencher nonetheless teaches the particular use of a hard drive 90 of Figure 2 within the encoder and decoder computer system and it is considered obvious that such hard drive memory of Vainsencher may certainly be used for storing the motion vectors in place of the SDRAM memory. The Examiner wants to further point out that: One of ordinary skill in the art is presumed to possess a certain amount of background knowledge independent of the references. In re Sovish, 769 F.2d 738, 226 USPQ 771 (Fed. Cir. 1985); In re Jacoby, 309 F.2d 513, 135 USPQ 317 (C.C.P.A. 1962). The conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference. In re Bozek, 416 F.2d 1385, 163 USPQ 545 (C.C.P.A. 1969). With this in mind, it is submitted that it is considered obvious to provide any suitable and commercially available memory device for storing any desired data, including the use of the hard drive 90 of Vainsencher for storing the motion vectors over the SDRAM 112 of Vainsencher so as to build frames of video data, and thereby rendering obvious the claimed invention.

Regarding the appellant's arguments at page 23 of the Brief filed September 27, 2005 concerning the rejection of claim 61, and in general that the combined Boyce, Takahashi and Mogeat references fail to disclose or suggest each and every limitation recited by claim 61 at least by virtue of its dependency from claim 1, the Examiner wants to point out that such arguments have been addressed in the above.

Art Unit: 2613

The appellant's argued at page 24 of the Brief filed September 27, 2005 the rejection of claim 10 under 35 USC 112, and in general that the indefinite rejection should be withdrawn on the grounds that the recitation of MPEG should be limited to those variations of MPEG known at the time of filing, and that the Office is requested to reconsider its position that one of ordinary skill in the art could readily determine that specific MPEG recommendation versions with a date based on the filing date of the present application. It is however again that it is conceivable to have various versions of the MPEG standard between the time the invention was reduced to practice and the time of filing. And unless the appellant provides a dated MPEG version, the metes and bounds of the claimed limitation have not be clearly identified and thus rendering the claim indefinite.

(11) Related Proceeding(s) Appendix

The appellant had failed to provide a Related Proceeding(s) Appendix section in the Brief filed September 27, 2005, as required by 37 CFR 41.37(c). But it is clear from the record that there is no decision rendered by a court or the Board in any proceeding, and therefore it is assumed that the appellant meant to include a statement of "NONE".

Art Unit: 2613

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,


RICHARD LEE
PATENT EXAMINER

Richard Lee/r1

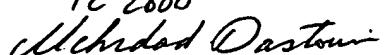
01/04/06

Conferees:

Mehrdad Dastouri

Chris Kelley

MEHRDAD DASTOURI
SUPERVISORY PATENT EXAMINER

TC 2600



CHRIS KELLEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600